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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,364	06/26/2003	Kyoung-Moon Lim	0630-1717P	4532

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EXAMINER	
SHANKAR, VIJAY	
ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,364	LIM, KYOUNG-MOON	
	Examiner	Art Unit	
	VIJAY SHANKAR	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,16,17 and 19-21* is/are rejected.

7)☒ Claim(s) *5-15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 16-17, 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al (US 2001/0048408) .

Regarding Claim 1, Koyama et al teaches a driving circuit for a flat panel display (fig.1), the circuit comprising: a latch unit (see Figures 26-27; Paragraph 9-21, 52) to which a control signal is applied from a shift register (see Figures 26-27; Paragraph 9-21, 52) to sample at least one digital picture signal and to store the digital picture signal (see Figures 26-27; Paragraph 8-21, 52-59, 95-97), and the latch unit simultaneously outputting the sampled picture signals by a line pass signal (Fig.,3, 26-27; Paragraph 8-21, 50-67; 71-87; 89-97); and a voltage to current converting unit (see Figures 19A-B; Paragraph 92-97, 187-208) supplying current of a plurality of

levels to a data line of the display panel according to logical combinations of the sampled picture signal from the latch unit, using a current mirror (see Figures 19, 24; Paragraph 200-208, 223-224) method (figs.1,3,9-10; Paragraph 0095-0107, 0182-0208, 0222-0225).

Regarding Claim 2, Koyama et al teaches a circuit wherein the latch unit comprises: a first latch unit being applied the control signal from the shift register to sample and store a digital picture signal having a plurality of bit numbers (see Figures 26-27; Paragraph 9-21, 52); and a second latch unit outputting the digital picture signal sampled in the first latch unit simultaneously according to an outer line-pass signal. (figs.1,3,10; Paragraph 9-21, 0050-0067; 0071-0087).

Regarding Claim 3, Koyama et al teaches a circuit wherein the shift register, the latch unit and the voltage to current converting unit are formed in the display panel. (fig.1; Paragraph 0050-0067; 0071-0087).

Regarding Claim 4, Koyama et al teaches a circuit wherein the display panel is an organic electroluminescence display panel. (Paragraph 0193-0194, 0197).

Regarding Claims 16-17, Koyama et al teaches the circuit wherein the voltage to current converting unit includes a current mirror with plurality of current paths. (see Figures 19A-B; Paragraph 92-97, 187-208).

Regarding Claim 19, Koyama et al teaches the flat panel display, comprising: a substrate; a plurality of pixel units located on the substrate; and a data driving circuit located on the same substrate, the data driving circuit including a plurality of current paths, the data driving circuit supplying current of a plurality of levels to at least one of the plurality of pixel units by providing the current from at least one of the plurality of current paths.

Regarding Claim 20, Koyama et al teaches the flat panel display wherein the data driving circuit includes a current mirror structure on the same substrate, the current mirror structure receiving a reference current to provide the current from the at least one of the plurality of current paths based upon logical combinations of bits of a digital picture signal. (see Figures 19A-B; Paragraph 92-97, 187-208).

Regarding Claim 21, Koyama et al teaches the flat panel display is an organic electroluminescence display (Paragraph 190-197).

Allowable Subject Matter

4. Claims 5-15 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance: The prior arts fail to teach a driving circuit for a flat panel display wherein the voltage to current converting unit comprises: a first switching unit for controlling a flow of a reference current by an enable signal; a second switching unit connected to the first switching unit for controlling the flow of the reference signal by the enable signal; a first NMOS transistor for forming a reference path on which the reference current flows between the first switching unit and ground by being applied the reference current on a gate electrode thereof; a plurality of NMOS transistors not including the first NMOS transistor for forming a plurality of current paths in a parallel direction between the data line and the ground of the display panel according to picture signals having a plurality of bit numbers by being applied the reference signal on respective gate electrodes thereof; and a plurality of switching units for controlling switching of the plurality of current paths by being applied the picture signal having the plurality of bit numbers independently as claimed in Claim 5 and 18.

Also, Claims 6-15 are allowable because it depends on Claim 5.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments filed 11-10-2005 have been fully considered but they are not persuasive.

Applicant argues that Koyama does not teach a current mirror method to supply current of a plurality of levels to a data line of the display panel according to logical combinations of the sampled picture signal from the latch unit, using a current mirror method .

However, Koyama does teach a current mirror method (see Figures 19, 24; Paragraph 200-208, 223-224) to supply current of a plurality of levels to a data line of the display panel according to logical combinations of the sampled picture signal from the latch unit, using a current mirror method (figs.1,3,9-10; Paragraph 0095-0107, 0182-0208, 0222-0225).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIJAY SHANKAR
Primary Examiner
Art Unit 2673

VS